AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A data input/output buffer[[,]] comprising:

~~a plurality of switching elements and a plurality of logical elements, wherein an NMOS transistor of a switching element driven according to a data signal inputted from a peripheral circuit or a logical element to which the data signal is inputted, of the plurality of the switching elements or the plurality of the logical elements, is a low voltage-driven NMOS transistor~~

a PMOS transistor driven according to the data signal which is directly inputted to the PMOS transistor from a peripheral circuit and connected to a power supply voltage terminal;

a low voltage-driven NMOS transistor driven according to the data signal which is directly inputted to the low voltage-driven NMOS transistor from the peripheral circuit and connected to the PMOS transistor, wherein the low voltage-driven NMOS transistor having a threshold voltage of 0V;

a NMOS transistor connected between the low voltage-driven NMOS transistor and a ground voltage terminal, wherein the NMOS transistor is turned on according to an output enable signal; and

a latch unit for inverting and restoring a signal received via the PMOS transistor or the low voltage-driven NMOS transistor.

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Currently Amended) A data input/output buffer[[,]] comprising:

a first logical element driven according to a data signal directly inputted to the first logical element from a peripheral circuit, the first logical element having a PMOS transistor and a low voltage-driven NMOS transistor; ~~and~~

a second logical element for ~~latching an output signal of the first logical element~~ inverting and restoring a signal received via the PMOS transistor or the low voltage-driven NMOS transistor; and

a NMOS transistor that is connected between the low voltage-driven NMOS transistor and a ground voltage terminal with the switching element being turned on according to an output enable signal,

wherein the low voltage-driven NMOS transistor having a threshold voltage of 0V.

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Currently Amended) A semiconductor memory device, comprising:

a memory cell array;

a row decoder for selecting a given page of the memory cell array according to a row address signal;

a page buffer for storing data stored at the page selected by the row decoder;

a column decoder for generating a bit line select signal according to a column address signal;

a column multiplexer for selecting and outputting any one of the data stored at the page buffer according to the bit line select signal; and

a data input/output buffer for storing the data selected by the column multiplexer and transferring the data to a data line, wherein ~~a device driven by the data is a low voltage-driven NMOS transistor~~ the data input/output buffer comprises a PMOS transistor driven according to the data signal directly inputted to the PMOS transistor from the column multiplexer and connected to a power supply voltage terminal;

a low voltage-driven NMOS transistor driven according to the data signal directly inputted to the low voltage-driven NMOS transistor from the column multiplexer and connected to the PMOS transistor, wherein the low voltage-driven NMOS transistor having a threshold voltage of 0V;

a NMOS transistor connected between the low voltage-driven NMOS transistor and a ground voltage terminal, wherein the NMOS transistor is turned on according to an output enable signal; and

a latch unit for inverting and restoring a signal received via the PMOS transistor or the low voltage-driven NMOS transistor.

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)